Design Example Using the altlvds Megafunction & the External PLL Option in Stratix II Devices

March 2006, ver. 1.0 Application Note 409

Introduction

The `altlvds` megafunction allows you to instantiate an external phase-locked loop (PLL) when using Stratix® II, HardCopy® II, or Cyclone™ II devices. This external PLL is a fast PLL set-up in LVDS mode. This option gives you more control over the PLL settings, and gives you access to PLL options such as bandwidth and dynamic reconfiguration, which are unavailable when instantiating the serializer/deserializer (SERDES) circuitry using the `altlvds` megafunction.

If you are not using the specialized PLL features, the external PLL option provides no benefit and should not be used with the `altlvds` megafunction.

Quartus II Project

The project discussed in this application note contains a complete design illustrating the connections between the external fast PLL and the `altlvds` receive megafunctions. A complete ModelSim® project, including simulation files demonstrating the functionality of the design, is available on the Altera® website.

Download the Design Files

The design files for this example are available on the Altera website, on both the literature page and the PLL & Clocking Design Examples page located at **http://www.altera.com/support/examples/functionality/pll-clocking.html**.

The example in these design files uses the LVDS receiver in the external PLL mode.

Example

The following example uses the MegaWizard® Plug-In Manager in the Quartus® II software to generate the `altpll` and `altlvds` megafunctions.

In this example, you will perform the following activities:

- Generate a high-speed differential receiver using the altlvds megafunction and the MegaWizard Plug-In Manager
- Generate the PLL using the MegaWizard Plug-In Manager
- Simulate the high-speed differential interface design using ModelSim

Design Details

This design consists of two megafunctions, altpll and altlvds. The function of this design is to convert four serial input channels into a 32-bit wide output bus with a deserialization factor of eight. The idea of this design is to show how to use the altlvds megafunction with an external PLL, as well as the altpll and the altlvds megafunction settings necessary for the correct operation. Refer to Table 1 for design specifications.

Table 1. Design Specifications

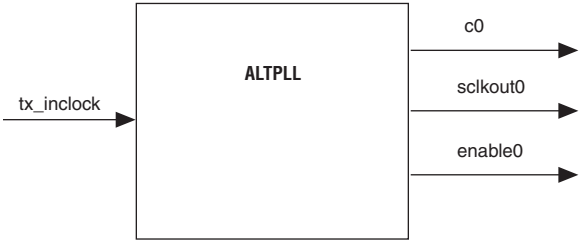
Specification	Inputs	Outputs	Details
altlvds	rx_datain[4:0], data rate 800 Mb/s	rx_out[31:0]	No built-in PLL

altpll	tx_inclock = 100 MHz	c0 = 100 MHz, // Core Clock
		sclkout0 = 800 MHz = data rate
		enable0 = enable pulse
			The enable pulse is generated once in 10 ns because the enable pulse period corresponds to the bigger of the two clock periods of core clock and sclkout0.*(1)*

Note to Table 1:
(1) sclkout0 is at a -180 degree phase shift to the VCO clock.

PLL inputs and outputs are shown in Figure 1.

Figure 1. PLL Inputs & Outputs



Generate an altlvds Receiver

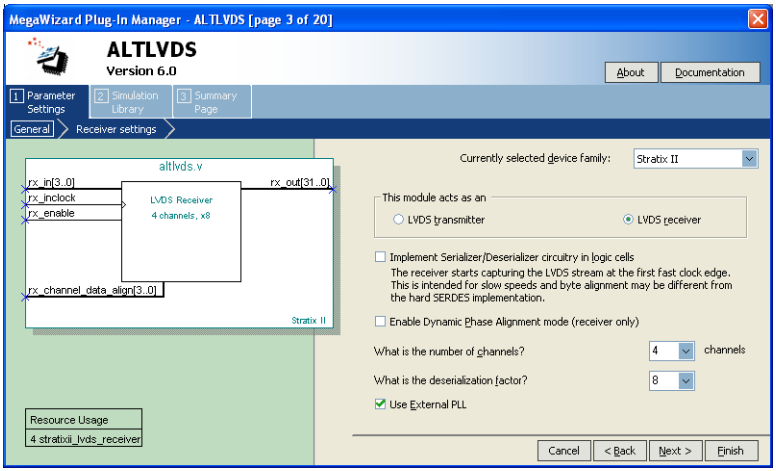
This section describes how to generate the `altlvds` and `altpll` megafunctions to generate an `altlvds` receiver using the MegaWizard Plug-In Manager.

1. Start the Quartus II software. On the Tools menu, click **MegaWizard Plug-In Manager**. Page 1 is shown.

2. Select **Create a new custom megafunction variation**, and click **Next**. Page 2a is shown.

3. On page 2a, in the **Installed Plug-Ins** list under **I/O**, select **ALTLVDS**. In the **Which device family will you be using?** list, select Stratix II. In the **What name do you want for the output file?** field, type the name of the output file. Select the output file type. Click **Next**. Page 3 is shown (Figure 2).

Figure 2. MegaWizard Plug-in Manager—ALTLVDS, Page 3

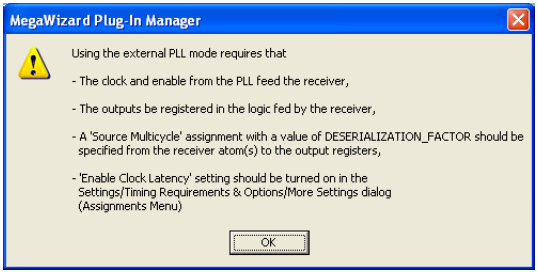


4. In the **Currently selected device family** list, select **Stratix II**.

5. Under **This module acts as an**, select **LVDS receiver**.

6. Turn on **Use External PLL**. This option is necessary if you want to take advantage of the Stratix II fast PLL features not accessible through the `altlvds` wizard. When you turn on this option, a warning dialog box is shown (Figure 3).

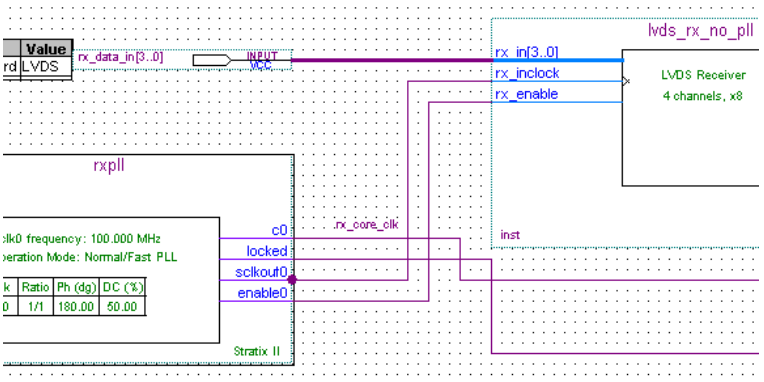
Figure 3. MegaWizard Plug-In Manager, Warning Dialog Box



This warning dialog box displays a list of requirements necessary to take advantage of the Stratix II fast PLL features. Selecting not to register the outputs of the receiver requires the following:

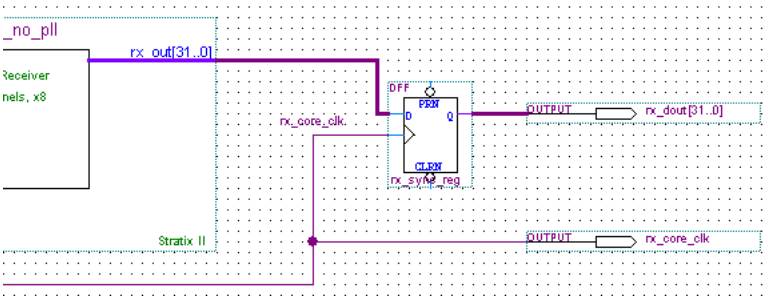
a. **The clock and enable from the PLL feed the receiver**—the output pins `sclkout0` and `enable0` of the PLL drive the input pins `rx_inclock` and `rx_enable` of the `altlvds` megafunction (Figure 4).

Figure 4. Connection Between altpll & altlvds



b. **The outputs are registered in the logic fed by the receiver**—the outputs must be pre-registered in the logic fed by the receiver in the connection between `altpll` and `altlvds`. Figure 5 shows the synchronization registers (`rx_sync_reg`) added at the receiver output.

Figure 5. Synchronization of the Output from altlvds Using Sync Registers

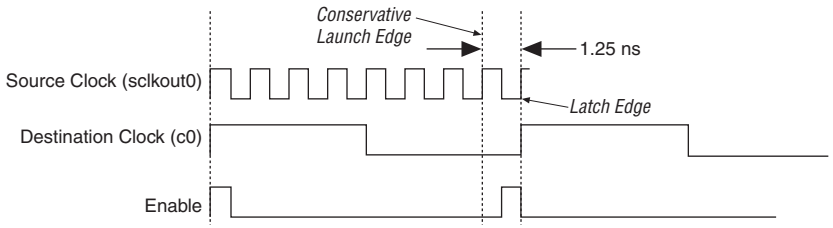


c. **A 'Source Multicycle' assignment with a value of DESERIALIZATION_FACTOR should be specified from the receiver atom(s) to the output registers**—specify a source multicycle assignment with a value of DESERIALIZATION_FACTOR from the receiver atoms (`rx_out`) to the output registers (`rx_sync_reg`).

Without the multicycle assignment, the Quartus II timing analyzer performs the timing analysis with overly conservative numbers, as the data is transferred from the high-speed transmitter clock to slow-speed synchronization registers.

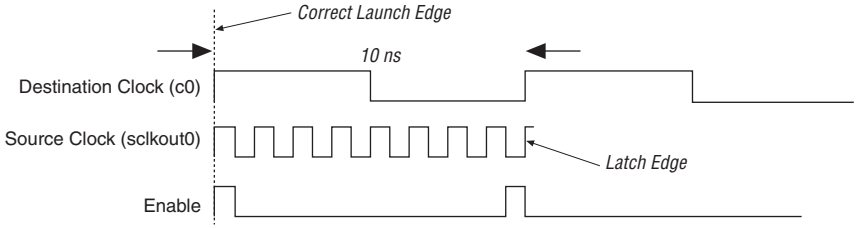
The `rx_out` data is clocked by the fast clock `sclkout0` at 800 MHz, or with a period of 1.25 ns. The sync registers are clocked by the slow clock `core_clock0` at 100 MHz, or a period of 10 ns. By default, the Quartus II timing analyzer assumes that data is launched and latched on consecutive active clock edges (Figure 6).

Figure 6. Overly Conservative Timing Estimate



As illustrated in Figure 6, the Quartus II software analyzes the design by taking only 1.25 ns for the data transfer between the output of `altlvds` and the sync registers. This is overly conservative because the enable pulse guarantees that only one of the high-speed transmitter clock edges are relevant in any given low-speed core clock period. To correct this, you must add a multicycle timing assignment to the Quartus II software, indicating which edges the timing analyzer must use (Figure 7).

Figure 7. Selection of the Proper Launch & Latch Edges



To set up the multicycle value, use the following formula:

`set_instance_assignment -name SOURCE_MULTICYCLE` *<DESERIALIZATION FACTOR>* `-from` *<register name>* `-to` *<register name>*

d. **'Enable Clock Latency' setting should be turned on in the Settings/Timing Requirements & Options/More Settings dialog (Assignments Menu)**—for the purpose of using `altlvds` in the external PLL mode, the clock latency setting must be on. There are two types of clock latency settings:

- Early Clock Latency
- Late Clock Latency

Refer to the Quartus II Help for additional information on the clock latency settings and their application.

7. In the warning dialog box, click **OK**.

8. On Page 3, in the **What is the number of channels?** list, select or type the desired number of channels (if a number is not listed, you can type the desired number of channels). In this example, enter **4** for the number of serial data channels.

Refer to the *Stratix II Device Handbook* for channel limitations for your target device size.

9. In the **What is the deserialization factor?** list, select the desired deserialization factor number. In this example, enter a deserialization factor (J factor) of **8**. The deserialization factors available in the list are device-family dependent. Click **Next**. Page 4 is shown.

10. Leave the settings in their default state and click **Next**. Page 5 is shown.

11. On Page 5, click **Finish**.

The `altlvds` module is built.

Generating an altpll Megafunction

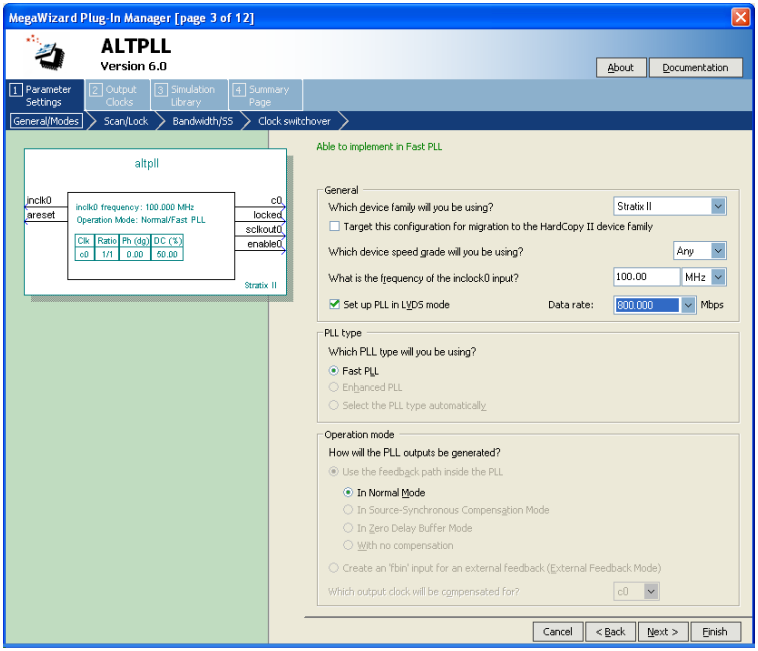
This section describes how to generate the `altpll` megafunction.

1. Start the Quartus II software. On the Tools menu, click **MegaWizard Plug-In Manager**. Page 1 is shown.

2. Select **Create a new custom megafunction variation** and click **Next**. Page 2a is shown.

3. On page 2a, in the **Installed Plug-Ins** list under **I/O**, select **ALTPLL**. In the **Which device family will you be using?** list, select **Stratix II**. In the **What name do you want for the output file?** field, type the name of the output file. Select the output file type. Click **Next**. Page 3 is shown (Figure 8).

Figure 8. MegaWizard Plug-in Manager—ALTPLL, Page 3



4. In the **Which device family will you be using?** list, select **Stratix II**.

5. In the **What is the frequency of the inclock0 input?** list, type `100.00` and select **MHz**.

   A frequency of 800 MHz for `sclkout0` can also be produced for an input frequency of 200 MHz. The `sclkout0` frequency is 800 MHz because the required data rate is 800 Mb/s.

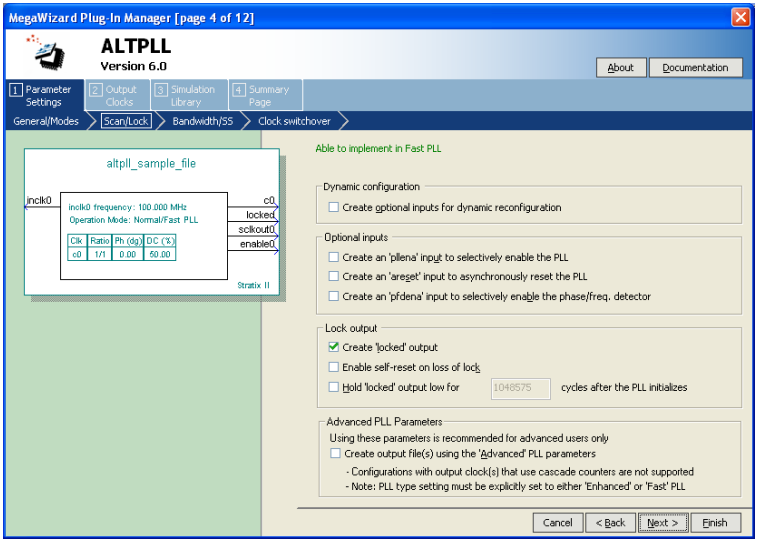
6. Turn on **Set up PLL in LVDS mode**, and in the **Data rate** list, select **800.00** Mbps.

7. Under **Which PLL type will you be using?**, **Fast PLL** is automatically selected.

   When the PLL is set up in the LVDS mode, fast PLL is the only option available.

8. Click **Next**. Page 4 is shown (Figure 9).

Figure 9. MegaWizard Plug-in Manager—ALTPLL, Page 4

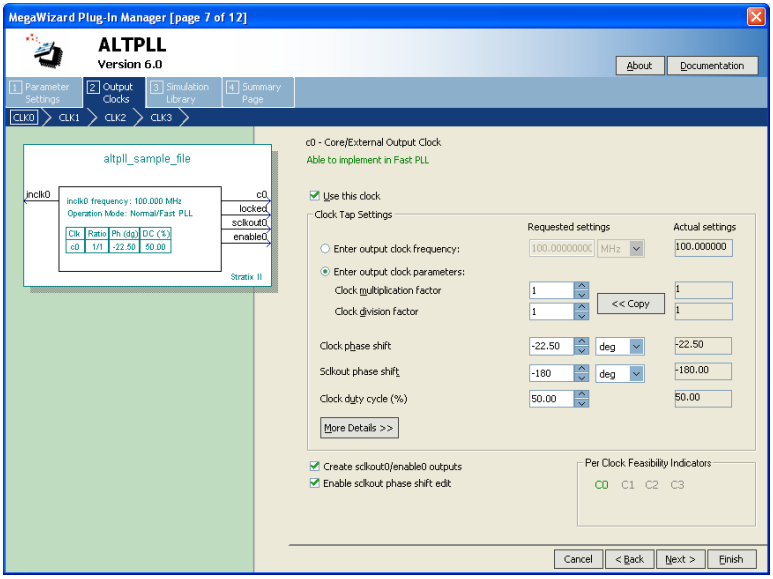


9. Under **Dynamic configuration**, turn off **Create optional inputs for dynamic reconfiguration**. Under **Optional inputs**, turn off all of the options. **Under Lock output**, turn on **Create 'locked' output**, and turn off **Enable self-reset on loss of lock** and **Hold 'locked' output low**. Under **Advanced PLL Parameters**, turn off **Create output file(s) using the 'Advanced' PLL parameters**. Click **Next**. Page 5 is shown.

10. On Page 5, leave the settings in their default state and click **Next**. Page 6 is shown.

11. On Page 6, leave the settings in their default state and click **Next**. Page 7 is shown (Figure 10).

Figure 10. MegaWizard Plug-in Manager —ALTPLL, Page 7



12. Turn on **Use this clock**.

13. Under **Clock Tap Settings**, select **Enter output clock parameters**. For **Clock multiplication factor**, type `1`. For **Clock division factor**, type `1`.

14. Turn on **Create sclkout0/enable0 outputs**, and turn on **Enable sclkout phase shift edit**.

15. Under **Clock Tap Settings**, for **Clock phase shift**, enter `-22.50`, and select **deg**. For the **Sclkout phase shift**, enter `-180` and select **deg**. For **Clock duty cycle (%)**, enter `50.00`.

The phase shift of the output clock `sclkout0` is set to -180 degrees with respect to the VCO clock.
The core clock phase shift is set to -22.5 degrees. This is calculated by dividing the `sclkout` phase shift by the clock multiplication factor of 8, as shown in Equation 1:

(1)

`sclkout0` frequency = input clock * 8
clock phase shift = 180/8 = 22.5 degrees

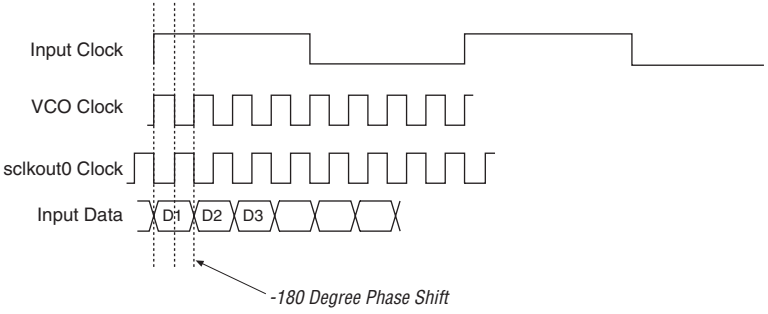
For more information about the relationship between VCO clock and the PLL output clocks, refer to the *Enhanced PLL Hardware Overview* section in the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*.

16. Click **Next**. Page 8 is shown.
17. On Page 8, leave the settings in their default state and click **Next**. Page 9 is shown.
18. On Page 9, leave the settings in their default state and click **Next**. Page 10 is shown.
19. On Page 10, leave the settings in their default state and click **Next**. Page 11 is shown.
20. On Page 11, click **Finish**.

The `altpll` module is built.

The advantage of introducing phase shift is to make sure that input data is captured properly as the data appears at the `altlvds` pin before the rising edge of the `sclkout0` as shown in the Figure 11.

Figure 11. Advantage of Introducing Phase Shift *Note (1)*



Note to Figure 11:
(1) It is assumed that data and clock are edge-aligned. If this is not true, adjust the phase shift.

Simulation

You can use the design file lvds_pll.zip to simulate the design. The lvds_pII.zip file contains the following files:

- **Quartus_stratixii_extpll.zip**. This file contains the Quartus II project.
- **Sim_stratixii_extpll_rtl.zip**. This file contains the script files to simulate the gate-level netlist using ModelSim. The gate-level netlist is generated using the Quartus II software, version 5.1, and the simulation models should refer to the Quartus II software, version 5.1. The following three script files are located in the directory:
  - **comp_altera_lib.do**. Use this file to compile the Altera library files for Stratix II components.
  - **comp_gate.do**. Use this file to compile the gate-level netlist and the testbench.
  - **sim.do**. Use this file to load the library and the design to ModelSim, and run the design.

To simulate the RTL netlist using ModelSim, use the script files contained in the following file located in your simulation directory:

- **Sim_stratixii_extpll_rtl.zip**. This file contains the script files to simulate the RTL netlist using ModelSim.
  - **comp_altera_lib.do**. This file compiles the Altera library files for Stratix II components.
  - **comp_rtl.do**. This file compiles the rtl-level netlist and the testbench.
  - **sim.do**. This file loads the library and the design to ModelSim, and runs the design.

For additional information, refer to the *altlvds Megafunction User Guide*, the *altpll Megafunction User Guide*, and the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*, available on the Altera website: www.altera.com.